REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary Zahn

CHECKED BY
Michael C. Jones

APPROVED BY
Alan Barone

DRAWING APPROVAL DATE
92-08-18

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 16-BIT, MICROPROCESSOR COMPATIBLE, D/A CONVERTER, HYBRID

SIZE	CAGE CODE	
A	**67268**	**5962-89862**

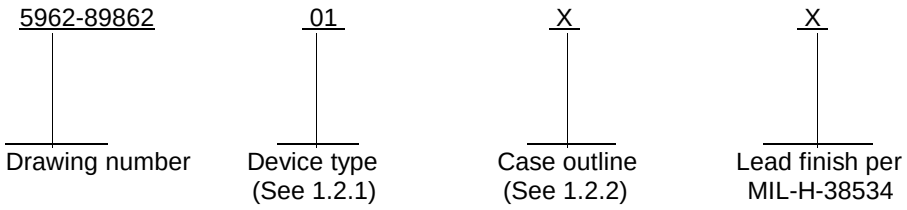
SHEET 1 OF 15

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-H-38534.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS9378TB	16-bit D/A converter, (16-bit linearity)
02	HS9378SB	16-bit D/A converter, (15-bit linearity)

1.2.2 Case outline(s). The case outline(s) shall be as designated MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28	28	Dual-in-line

1.3 Absolute maximum ratings.

Positive supply voltage (V_{CC})	+17 V dc
Negative supply voltage (V_{EE})	-22 V dc
Logic inputs to logic ground	5.7 V dc
Analog inputs to analog ground:	
Pins 10 and 12	V_{EE} to V_{CC}
Pin 11	-9.0 V dc to +V_{CC}
Pin 13	±0.1 V dc
Output voltage (V_{OUT})	Indefinite short circuit to GND
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	600 mW
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Positive supply voltage range	+14.25 V dc to +15.75 V dc
Negative supply voltage range	-14.25 V dc to -15.75 V
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standards. Unless otherwise specified, the following specification and standards of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-H-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

(Copies of the specification and standards required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-H-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-H-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.5 Unipolar and bipolar code table(s). The unipolar and bipolar code table(s) shall be as specified on figure 4.

3.2.6 Functional diagram(s). The functional diagram(s) shall be as specified on figure 5.

3.2.7 Timing diagram(s). The timing diagram(s) shall be as specified on figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-H-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534 (see 6.6 herein).

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-H-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DESC-EC) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in QML-38534 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-H-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-H-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-H-38534.

4.2 Screening. Screening shall be in accordance with MIL-H-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specifiy the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DIGITAL INPUT:							
Low level input voltage	V_{IL}	1 TTL load 2/	1, 2, 3	All		0.8	V
High level input voltage	V_{IH}	1 TTL load 2/	1, 2, 3	All	2.4		V
Input current	I_{IN}	V_{IL} = 0 V, V_{IH} = 5 V 2/	1, 2, 3	All		10	µA
Setup time	t_s	3/ 4/	9, 10, 11	All	0		ns
Latch control pulse width	t_p	3/	9, 10, 11	All	100		ns
Data hold time	t_h	3/ 4/	9, 10, 11	All	100		ns
ANALOG OUTPUT:							
Scale factor error	SFe	5/	1	All	-0.20	+0.20	% FSR
			2, 3	01	-0.30	+0.30	
				02	-0.35	+0.35	
Initial offset unipolar	V_{OSU}	5/	1	All	-0.05	+0.05	% FSR
			2, 3	01	-0.07	+0.07	
				02	-0.10	+0.10	
Initial offset bipolar	V_{OSB}	5/	1	All	-0.10	+0.10	% FSR
			2, 3	01	-0.10	+0.10	
				02	-0.15	+0.15	
Output impedance	Z_{OUT}	3/	1	All		1.0	ohm

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
STATIC PERFORMANCE:							
Integral linearity error	ILE	6/	1	01		0.0015	% FSR
			2, 3			0.0115	
			1	02		0.003	
			2, 3			0.013	
Differential linearity error	DLE	7/	1	01		0.0015	% FSR
			2, 3			0.0115	
			1	02		0.003	
			2, 3			0.013	
Monotonicity	MON		1	01		16	BITS
			2, 3			15	
			1	02		15	
			2, 3			14	
POWER SUPPLY:							
Positive power supply current	I_{CC}	+14.25 V dc $\le V_{CC} \le$ +15.75 V dc	1, 2, 3	All		28.5	mA
Negative power supply current	I_{EE}	-14.25 V dc $\le V_{EE} \le$ -15.75 V dc	1, 2, 3	All	-11.5		mA
Rejection ratios	PSRR±		1, 2, 3	All	-0.002	+0.002	% FS/ % V_S
Functional test		See 4.3.1c	7, 8	All			

1/ Unless otherwise specified, +14.25 V dc $\le V_{CC} \le$ +15.75 V dc and -14.25 V dc $\le V_{EE} \le$ -15.75 V dc.
2/ Voltages at logic inputs may not go below 0 volts or exceed +5.0 V.
3/ Parameter shall be tested as part of device initial characterization and after design and process change. Parameter shall be guaranteed to limits specified in table I for all lots not specifically tested.
4/ t_S = setup time required for input data to be valid before $\overline{CS}$, LBE, or HBE going active, t_h = hold time for $\overline{CS}$ to stay low.
5/ Adjust to zero.
6/ Integral linearity is measured per end-point definition.
7/ Differential linearity error is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent codes.

Device types	01 and 02	Device types	01 and 02
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Bit 1 (MSB)	15	-15 V dc (V_{EE})
2	Bit 2	16	+15 V dc (V_{CC})
3	Bit 3	17	GND
4	Bit 4	18	LBE
5	Bit 5	19	CS
6	Bit 6	20	HBE
7	Bit 7	21	Bit 16 (LSB)
8	Bit 8	22	Bit 15
9	LDAC	23	Bit 14
10	Gain adjust	24	Bit 13
11	Bipolar offset	25	Bit 12
12	Range	26	Bit 11
13	Summing junction	27	Bit 10
14	V_{OUT}	28	Bit 9

FIGURE 1. Terminal connections.

Device types 01 or 02 interfaced with 8-bit microprocessor

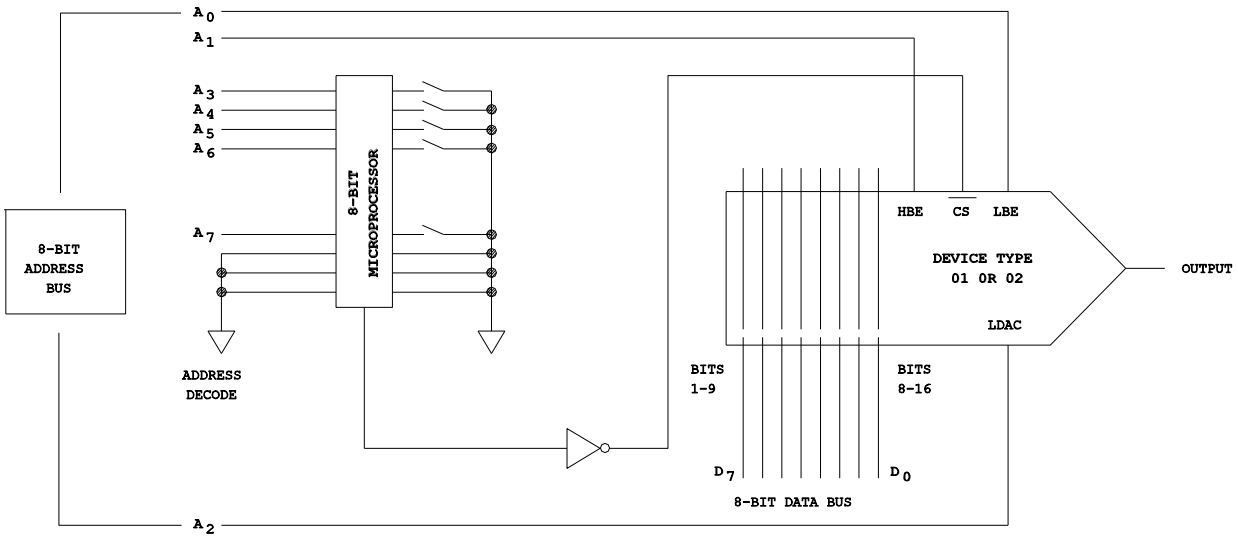


FIGURE 2. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**5962-89862**
		REVISION LEVEL	SHEET **8**

Control inputs

A_7 - A_3 (CS)	A_2 (LDAC)	A_1 (HBE)	A_0 (LBE)	Operation
Defined by switches to give low signal to CS when the device is addressed	0	0	0	All data latched
	0	0	1	Data into low byte of 1st buffer, all others latched
	0	1	0	Data into high byte of 1st buffer, all others latched
	0	1	1	Invalid address latched
	1	0	0	Data into 2nd buffer (16 bits) and D/A, 1st buffer latched
	1	0	1	Invalid address
	1	1	0	Invalid address
	1	1	1	Data directly to D/A from bus, latches transparent

A_{15} - A_2 (CS)	A_1 (LDAC)	A_0 (HBE, LBE)	Operation
Defined by switches to give low signal to CS when the device is addressed	0	0	Data latched
	0	1	Data into 1st buffer, 2nd buffer latched
	1	0	Data into 2nd buffer, 1st buffer latched
	1	1	Data directly to D/A, latches transparent

FIGURE 3. Truth table(s).

Unipolar

Binary input	Analog output
111 111	+F.S. -1 LSB
100 000	+F.S./2
011 111	+F.S./2 -1 LSB
000 000	0 V

Bipolar

Binary input	Analog output
111 111	+F.S. -1 LSB
100 000	0 V
011 111	-1 LSB
000 000	-F.S.

FIGURE 4. Unipolar and bipolar code table(s).

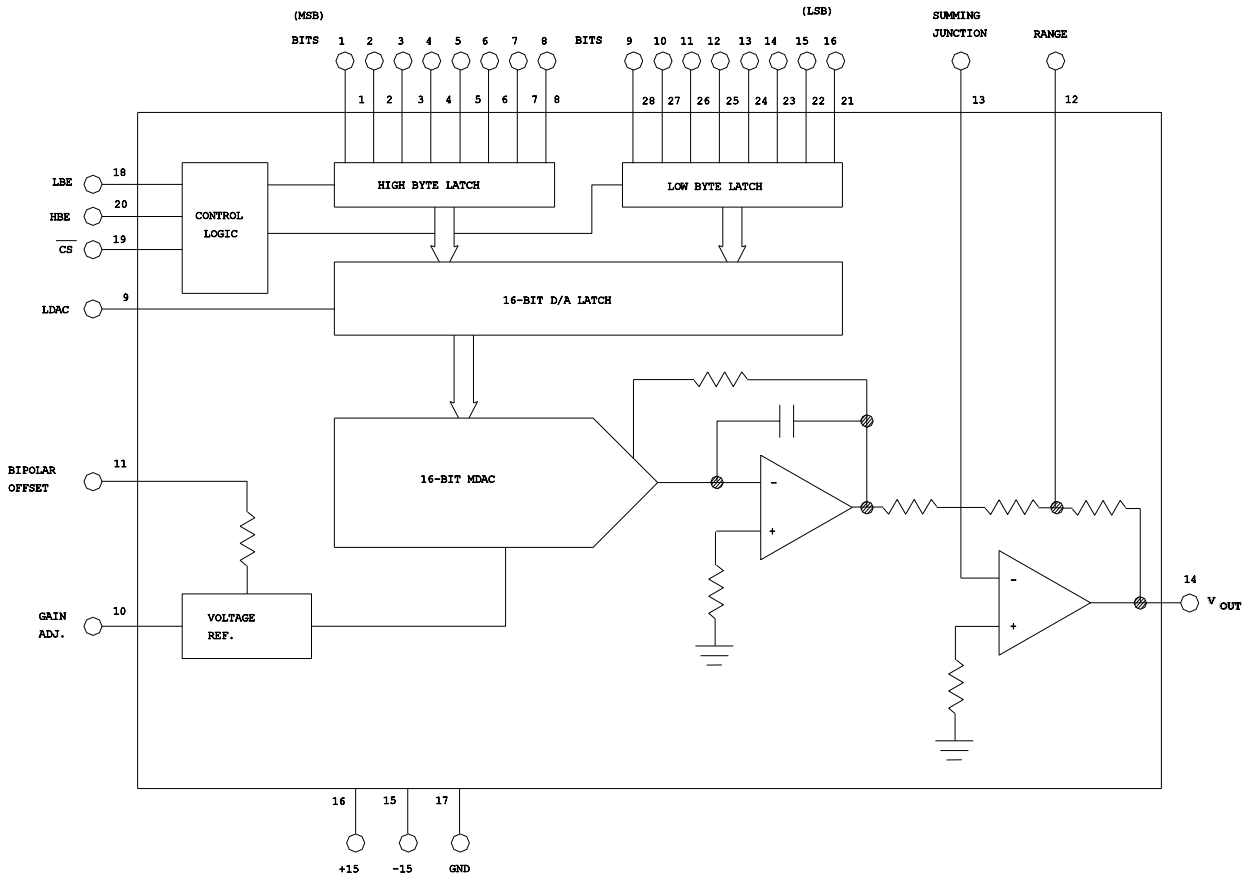
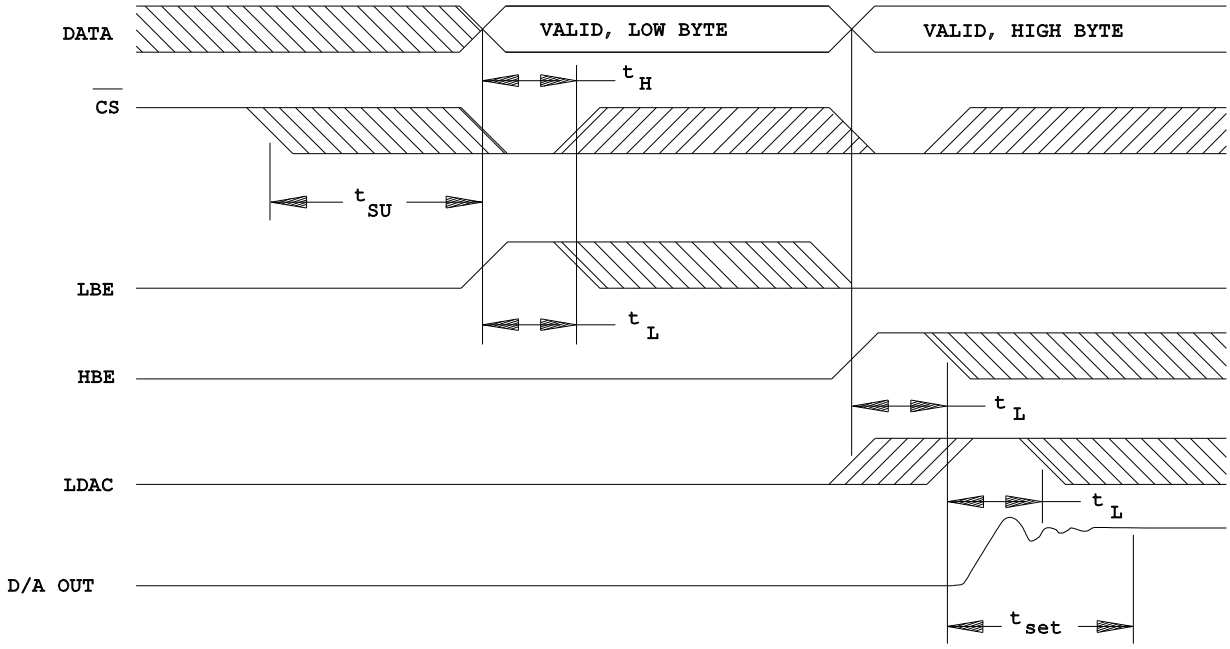


FIGURE 5. Functional diagram(s).

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**5962-89862**
		REVISION LEVEL	SHEET **11**

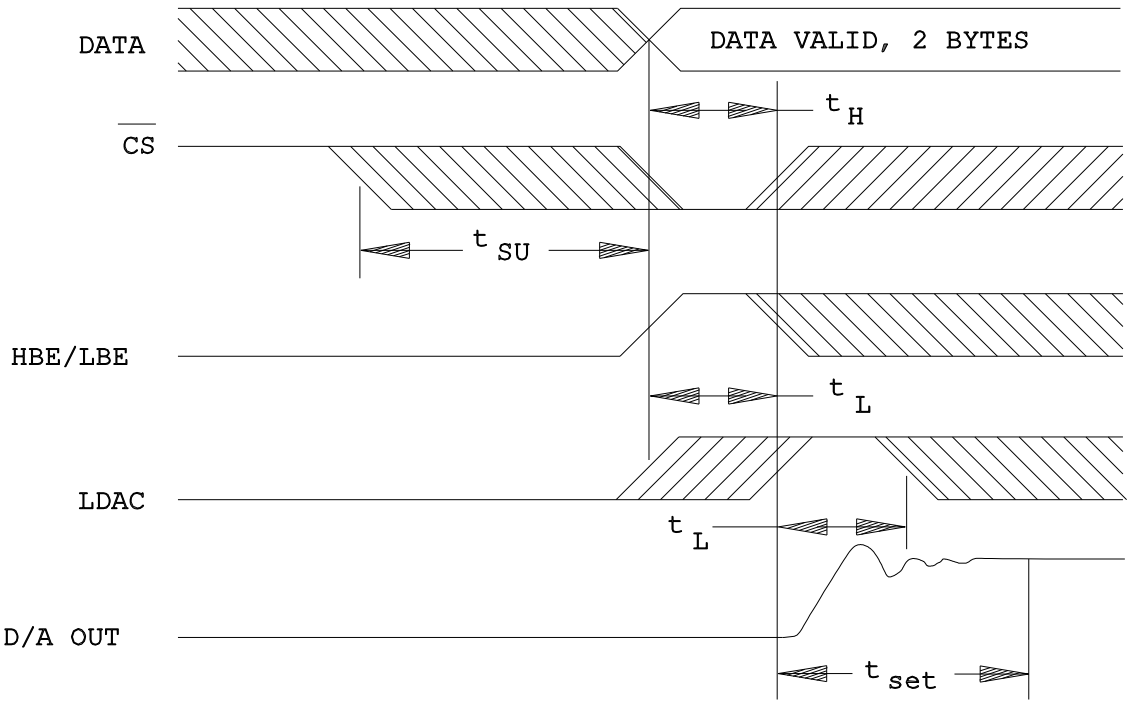
Interface to 8-bit microprocessor bus



NOTES:
1. t_{SU} setup time required for input data to be valid before CS, LBE, or HBE going active is 0 ns minimum.
2. t_H hold time for CS to stay low is 100 ns minimum.
3. t_L latch time for LBE, HBE, and LDAC is 100 ns minimum.
4. t_{SET} setting time from LDAC going active to valid output:
   a. 0.0015 percent F.S.R., all zeros to all ones is 22 µs.
   b. 0.0015 percent F.S.R., midscale LSB transition is 16 µs.

FIGURE 6. Timing diagram(s).

Interface to 16-bit microprocessor bus.



NOTES:
1. HBE and LBE are connected together.
2. t_{SU} setup time required for input data to be valid before $\overline{CS}$, LBE, or HBE going active is 0 ns minimum.
3. t_H hold time for $\overline{CS}$ to stay low is 100 ns minimum.
4. t_L latch time for LBE, HBE, and LDAC is 100 ns minimum.
5. t_{SET} setting time from LDAC going active to valid output:
   a. 0.0015 percent F.S.R., all zeros to all ones is 22 µs.
   b. 0.0015 percent F.S.R., midscale LSB transition is 16 µs.

FIGURE 6. Timing diagram(s) - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5008, group A test table)
Interim electrical parameters	1
Final electrical test parameters	1*, 2, 3, 7, 8, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-H-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-H-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. Subgroups 7 and 8 testing shall be sufficient to verify the truth table.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-H-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-H-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specifiy the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-H-38534.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-H-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for original equipment design applications and logistic support of existing equipment.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5373.

6.6 Approved sources of supply. Approved sources of supply are listed in QML-38534. Additional sources will be added to QML-38534 as they become available. The vendors listed in QML-38534 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-EC.